

Determination of Stability Using Return Ratios in Balanced Fully Differential Feedback Circuits

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Abstract— This paper describes SPICE [1] simulation techniques that can be used to find the return ratios for the differential and common-mode feedback loops in balanced, fully differential circuits. Since each of these loops may contain multiple feedback paths, conditions under which these two return ratios are sufficient for determining stability of the balanced feedback circuit are described. To allow the use of these techniques with switched-capacitor common-mode feedback circuits, a special simulation technique is presented that finds the dc bias for the return-ratio simulations.

I. INTRODUCTION

FULLY differential structures are often used in integrated circuits because they offer many advantages over their single-ended counterparts. Some of the advantages are improved immunity to power-supply noise, greater output voltage swing, and cancellation of even-order distortion. These benefits come at the expense of increased complexity.

Fig. 1 shows the schematic of a fully differential feedback amplifier. It consists of an operational amplifier (op amp), two input impedances, two feedback impedances, and two load impedances. It has two feedback paths: one from the positive op-amp output to the inverting op-amp input, and the other from the negative op-amp output to the noninverting op-amp input. Therefore, the circuit is an example of a multiple-loop feedback network. Determination of stability of multiple-loop feedback circuits through frequency-domain analysis is difficult in general [2]–[4]. If the structure is perfectly balanced, however, the analysis is simplified by using differential-mode (DM) and common-mode (CM) concepts [5], [6]. This is because DM signals do not give rise to CM signals (and vice versa) in a balanced structure. Furthermore, if the DM and CM feedback loops can be modeled as single-loop feedback circuits (which are defined in [2], [3]), frequency-domain stability analysis simplifies to finding one return ratio for each loop.

The return ratio associated with a controlled source is a measure of loop transmission in a single-loop feedback circuit [2], [3], [7], [8]. The return ratio is important because it can be used to check stability of the feedback circuit. Techniques that can be used in SPICE to simulate the return ratio of a

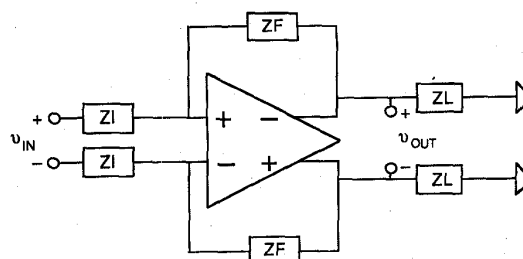


Fig. 1. An example of a fully differential feedback circuit.

single-loop feedback circuit have been reported previously [8]–[10]. These techniques were developed for single-ended amplifiers and are extended here to the perfectly balanced differential case. Because the DM and CM loops cannot always be modeled as single-loop feedback circuits, this paper also describes the conditions under which one return ratio for each loop is sufficient for determining the stability of the balanced feedback circuit. One important problem that arises in practice is that direct frequency-domain simulation of circuits that use switched-capacitor common-mode feedback is difficult because such feedback is inherently discrete in time. To overcome this problem, a special simulation technique for these circuits that finds the dc operating point during the return-ratio simulation is presented.

This paper is organized as follows. Basic assumptions are stated in Section II. The return-ratio concept is reviewed in Section III. In Section IV, conditions under which one return ratio is sufficient for determining stability of a multiple-loop circuit are described. Then the special case of switched-capacitor CM feedback loops is covered in Section V. An example is given in Section VI. Conclusions are presented in Section VII. Appendices A and B contain detailed proofs and derivations of key equations in Sections IV and V, respectively.

II. ASSUMPTIONS AND TERMINOLOGY

Unless stated otherwise, the following assumptions hold throughout this paper.

- 1) The differential circuit is perfectly symmetric [5], [11].
- 2) The feedback network has a unique dc operating point.
- 3) Every circuit under study can be reduced to a single-loop feedback circuit or to a multiple-loop circuit with a break point as described in Section IV.
- 4) The linear feedback network under analysis is composed of controlled sources and passive elements.

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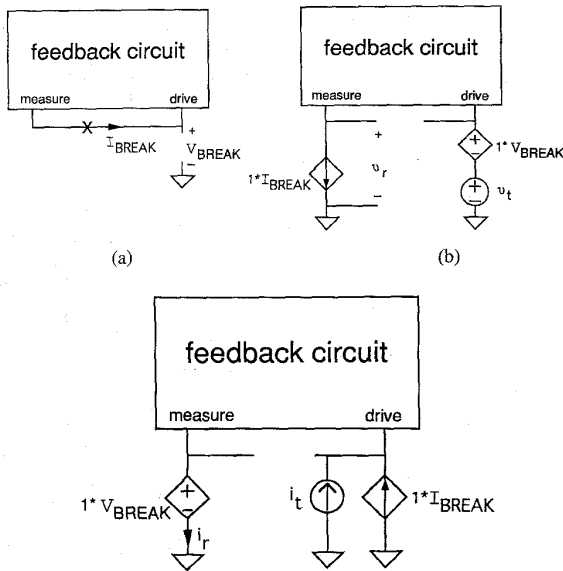


Fig. 2. Circuits for SPICE simulation of RR using replica biasing for a single-ended single-loop feedback circuit. (a) The dc reference circuit. (b) Circuit for measurement of RR_V . (c) Circuit for measurement of RR_I .

5) The term "stability" here refers to small-signal stability at the given dc operating point.

The IEEE standards for voltages and currents are observed in this paper; i.e., v_i is an ac voltage, V_I is a dc voltage, and v_I is a total (ac + dc) voltage.

III. BACKGROUND

The key characteristic of a single-loop feedback circuit is that there is a unique signal path that traverses the feedback loop from a dependent source in an active device to its controlling signal. The loop transmission of a single-loop transistor feedback circuit can be evaluated by computing the return ratio (RR) for a dependent source in an active device [2], [3], [7], [8]. The expression for the closed-loop gain G_{CL} in terms of RR is

$$G_{CL} = \frac{a}{1 + RR} + d, \quad (1)$$

where a is the forward gain through the dependent source and d is the forward transmission around the dependent source (that is, when the chosen dependent source is set to zero) [2], [8], [12]. Under the assumptions in Section II, the poles of $a(s)$, $d(s)$, and $RR(s)$ are in the left-half of the s plane [2], [8]. The presence of a right-half plane pole in G_{CL} can be discovered from a Nyquist plot of $RR(s)$ or from the gain and/or phase margins of $RR(s)$ [2], [3].

Techniques for finding the return ratio by using a combination of generalized voltage and current return ratios were presented in [9] and [10]. These methods are reviewed below and in Figs. 2–4, where the single-loop feedback circuit under simulation is drawn as a block with two terminals, labeled "drive" and "measure." Inside the feedback circuit, the signal flow is from the drive terminal to the measure terminal. When these terminals are connected together, the feedback loop is intact.

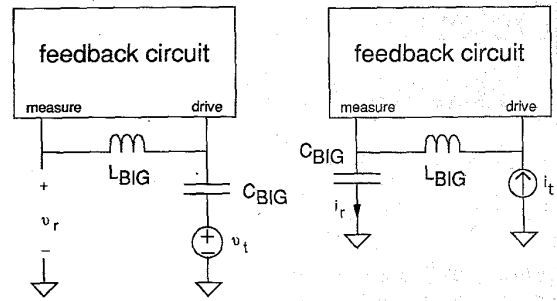


Fig. 3. Circuits for SPICE simulation of RR using inductors and capacitors at the break point. (a) Circuit for measurement of RR_V . (b) Circuit for measurement of RR_I .

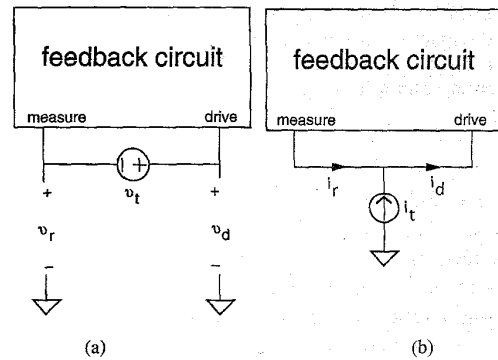


Fig. 4. Circuits for SPICE simulation of RR using ac signals that do not open the loop. (a) Circuit for measurement of RR_V . (b) Circuit for measurement of RR_I .

- 1) The return ratio of a single-loop feedback circuit can be found by breaking the circuit at an arbitrary point to find a voltage return ratio RR_V and current return ratio RR_I [9]. RR_V (RR_I) is found by setting all independent sources in the linearized small-signal circuit to zero, breaking the feedback loop, driving with a test voltage v_t (test current i_t), and measuring the return voltage v_r (return current i_r) appearing across an open circuit (flowing into a short circuit) at the other side of the break point. Then $RR_V = -v_r/v_t$ ($RR_I = -i_r/i_t$), and the total return ratio is given by

$$RR = \left[\frac{1}{RR_V} + \frac{1}{RR_I} \right]^{-1}. \quad (2)$$

A key problem with this approach is that breaking the feedback loop to inject the ac test signals disrupts the dc operating point. The closed-loop dc operating point can be preserved during simulation of RR_V and RR_I by using replica biasing [13], as illustrated in Fig. 2. Fig. 2(a) shows the dc reference circuit. It is a replica of the circuits used to find RR_V [Fig. 2(b)] and RR_I [Fig. 2(c)] before the loop is broken at the break point X. In Fig. 2(a), all independent ac sources are set to zero; the dc voltage from the break point to ground is V_{BREAK} , and the dc current flowing through the break point is I_{BREAK} . Controlled sources that depend on these quantities are used to reproduce the bias in

Fig. 2(b) and (c). To find the RR , the calculations in (2) can be carried out by post processing the SPICE output. The resulting RR is accurate for all frequencies.

One drawback of this approach is that breaking the feedback loop sometimes produces a node that has no dc path to ground because capacitors block all such paths at the break point. To overcome this problem, dc paths to ground can be introduced by adding negligibly large resistances from the breaks to ground. To make sure that the effect of the added resistances is properly incorporated into the dc bias point, these resistances should be added to all three simulation circuits [Fig. 2(a)–(c)]. One convenient way to do this is to enter the feedback network as a subcircuit that is used repeatedly for all simulations.

- 2) Large inductors and capacitors can be used to produce ac open and short circuits at the break point for ac simulation of RR_V and RR_I [8], [14]. Fig. 3(a) and (b) show circuits that use these elements to find RR_V and RR_I , respectively. The inductors and capacitors are connected so that the ac signals are injected and sensed without affecting the dc feedback loop. This approach uses (2) to find the RR for frequencies above a low-frequency limit that is determined by the size of the inductors, capacitors and circuit impedances.
- 3) Finally, the closed-loop dc operating point can be preserved by injecting the test signals without breaking the loop. (See method four in [10] or [15].) Fig. 4(a) shows that an ac test voltage source can be connected between the measure and drive terminals. From KVL, this injected test voltage sets the difference between the voltages v_d and v_r . These voltages can be used to find a voltage return ratio, $RR'_V = -v_r/v_d$. Similarly, Fig. 4(b) shows that an ac test current source can be connected from ground to a point that connects the measure and drive terminals. As shown, the test current divides into the currents i_r and i_d , which can be used to find a current return ratio, $RR'_I = -i_r/i_d$. Since the feedback loop is not broken during these simulations, RR'_V and RR'_I differ from RR_V and RR_I , respectively. To find RR , the following equation can be applied through post processing of the SPICE output.

$$\frac{1}{1 + RR} = \frac{1}{1 + RR'_V} + \frac{1}{1 + RR'_I}. \quad (3)$$

The ac test sources used here do not interfere with the dc bias. This approach requires the least complicated circuits but the most complicated calculation and may be numerically unstable when the phase margin is very small. To make the resulting RR as accurate as in method 1 for all frequencies, greater numerical precision is required here than there because the magnitudes of neither RR'_V nor RR'_I approach zero as the frequency approaches infinity in general. (Instead, these magnitudes become reciprocals in the limit with values that depend on the ratio of the impedances on the left and the right of the break [10].)

Any of these techniques can be extended to find the DM and CM return ratios in balanced fully differential feedback circuits by identifying two symmetrical break points that break both the DM and CM feedback loops [16]. If these breaks are driven by purely differential signals, only the DM loop is excited, and the differential voltage and current return ratios can be measured. Similarly, if the breaks are driven by purely CM signals, only the CM loop is excited and the CM return ratios can be measured. While the DM and CM return ratios are found through direct simulation of the balanced circuit, conditions under which these return ratios determine the stability of the balanced circuit are most easily described through the corresponding DM and CM half circuits. The simplest condition under which this is true is when the corresponding DM and CM half circuits are both single-loop feedback circuits. However, a key problem is that the DM and CM half circuits are often not single-loop feedback circuits. As a result, one return ratio for the DM loop and one for the CM loop are not always enough to determine stability of the original circuit. When one or both half circuits contain multiple feedback paths, other conditions exist under which these two return ratios are sufficient for determining stability of the balanced circuit. These conditions are described in the next section from the standpoint of single-ended, multiple-loop feedback circuits that could represent the DM or CM half circuits of balanced fully differential feedback circuits.

IV. MULTIPLE FEEDBACK LOOPS

In single-loop feedback circuits, stability can be checked by finding the gain and/or phase margins of a single return ratio. When multiple feedback loops are present, however, multiple return ratios must be examined under various conditions to check stability in general [2]–[4], [17]. In some special cases, however, stability of a multiple-loop circuit can be determined from a single return ratio. This section presents examples of multiple-loop feedback and also conditions under which the stability of a multiple-loop network can be determined from a single return ratio.

Fig. 5(a) shows an example feedback circuit that includes an op amp with a tail current source (MCS) that biases the input differential pair. Fig. 5(b) and (c) shows the corresponding DM and CM half circuits, respectively. The DM half circuit is a single-loop feedback network because the only feedback path is from the drain to the gate of M1 through ZF in parallel with $C_{gd}(M1)$. For simplicity, $C_{gd}(M1) = 0$ will be assumed at first. Nonzero $C_{gd}(M1)$ can be included as part of ZF or treated as a separate local feedback loop as described below. In contrast, the CM half circuit has multiple feedback loops because there is global feedback around the op amp as well as local feedback through the source degenerating impedance, $2Z_O(\text{MCS})$.

In many fully differential op amps, special circuits are used to control the common-mode output voltage, V_{OC} [18]. Fig. 6 shows an example in which there are two CM feedback loops. One loop is through the passive feedback network (e.g., ZF and ZI) and back to the outputs through M1 and M2. The second loop is through the CM-sense block (which consists of

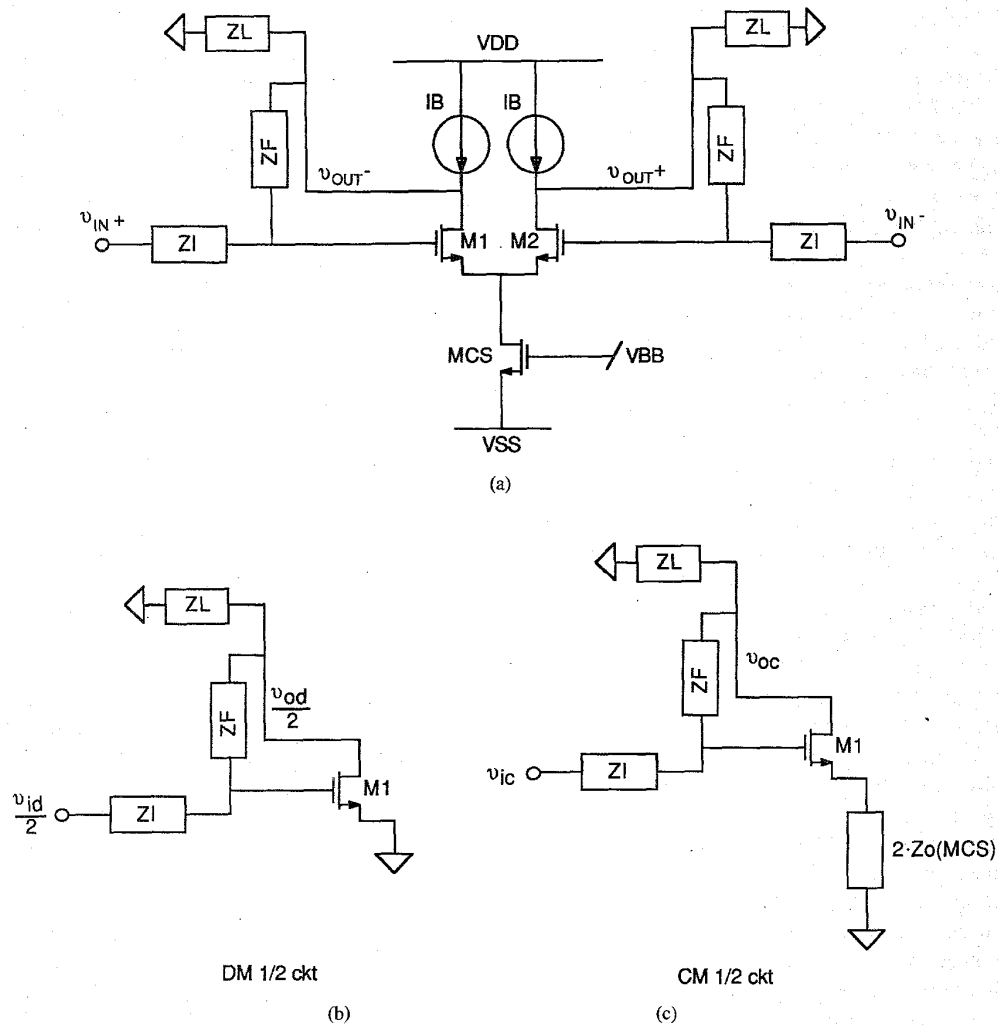


Fig. 5. (a) A feedback circuit that uses an op amp with current source biasing of the input differential pair. (b) The single-loop DM half circuit. (c) The multiple-loop CM half circuit.

the two impedances of value Z_{CM}) and back to the outputs through MCS, M1, and M2. In the remainder of this paper, loops similar to this second loop, where a CM-sense block is used to sense the CM output voltage, will be referred to as CMSFB (CM-sense feedback) networks.

If the DM half circuit is a single-loop feedback circuit, and if the structure is balanced, the presence of multiple CM feedback loops does not affect the simulation of $RR(DM)$. A similar statement can be made for the less common case of multiple DM feedback loops with a single CM feedback loop. To determine $RR(DM)$ in a circuit that contains a CMSFB loop, the break points can be chosen either to maintain or break the CMSFB loop. In Fig. 6(a), for example, the break points marked by the X's maintain the CMSFB loop while those marked by the large dots break this loop. Since the dc operating point is maintained, either approach is acceptable.

As noted above, multiple return ratios must be examined to determine the stability of a general multiloop network. Extension of RR simulation to general multiple-loop circuits is a topic that is open for investigation. In two special cases

that are presented next, however, the small-signal stability of a multiple-loop network can be determined based on a single return ratio.

The first special case applies to circuits with any number of local feedback loops inside one global feedback loop. This is referred to here as embedded local feedback. If each embedded local feedback loop is stable by itself, then stability can be checked by breaking the global feedback loop while keeping all the local feedback loops intact and calculating the gain and/or phase margins [19]. For example, Fig. 7(a) shows a signal-flow diagram for such a system with one local feedback loop, where g_{1-4} and f_{3-4} are stable (i.e., they have only left-half plane poles). The system is redrawn in Fig. 7(b) in the form of a single-loop system. If the g_{3-f3} loop is stable, system stability can be determined by breaking the global loop at the X.

This concept can be extended to feedback circuits as follows. If each embedded local feedback circuit can be modeled as a combination of a stable controlled source and input and output impedances that consist of only passive elements, the

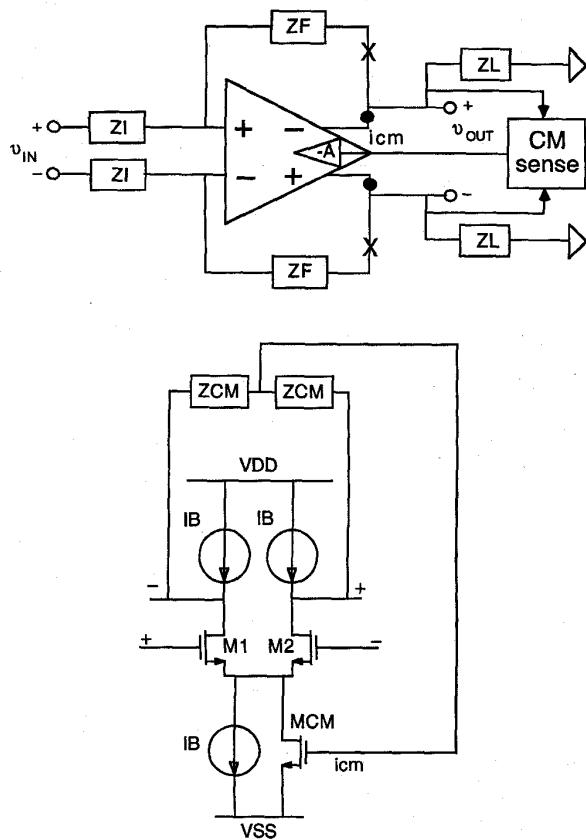


Fig. 6. (a) A fully differential feedback circuit using a CM sense feedback loop to control the CM output voltage. (b) The op amp in (a), including the CM sense feedback loop.

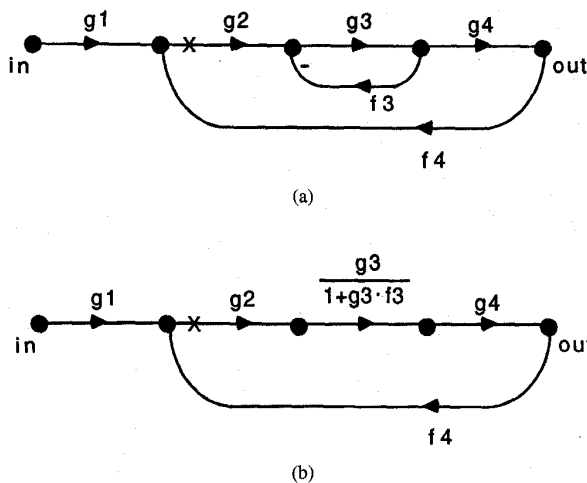


Fig. 7. (a) A multiple loop network with an embedded (or minor) loop. (b) (a) redrawn with the embedded loop replaced by an equivalent transfer function.

multiple-loop circuit reduces to a single-loop circuit. Then the stability can be checked by finding the RR at a break point that opens the global loop but leaves the local feedback loops intact. As an example, consider the three-stage feedback amplifier in Fig. 8. The first and third stages are each modeled

by three elements. By assumption, $G_{m1}(s)$ and $G_{m3}(s)$ are stable, and $Z_{in1}, Z_{in3}, Z_{out1}$, and Z_{out3} are passive networks. The second stage is a MOSFET gain stage that has local feedback around $M2$ provided by R_{F2} in parallel with C_{gd} of $M2$. If this second stage can be modeled in the same way as the other stages, with stable $G_{m2}(s)$ and passive $Z_{in2}(s)$ and $Z_{out2}(s)$, stability of the entire amplifier can be checked by breaking the circuit at a point that breaks the global loop but leaves the local loop intact (such as at the X in Fig. 8), and applying one of the RR simulation methods reviewed in Section III.

The requirement that $Z_{in2}(s)$ and $Z_{out2}(s)$ can be modeled by a connection of passive components (or, equivalently, that $Z_{in2}(s)$ and $Z_{out2}(s)$ are rational, positive real functions of s [20]) is overly restrictive. For instance, assume that Z_{out2} can be modeled by a $-1 \text{ M}\Omega$ resistor in parallel with a 10 pF capacitor. If Z_{in3} is a $200 \text{ k}\Omega$ resistor, then the parallel combination of Z_{in3} and Z_{out2} can be replaced by a purely passive network (i.e., $250 \text{ k}\Omega$ in parallel with 10 pF) and the resulting circuit satisfies the assumptions in Section II. Therefore, a less-restrictive condition on the impedances Z_{in2} and Z_{out2} is that they must yield a passive network when viewed in combination with the passive components to which they are connected.

The other special case of multiloop feedback applies to circuits in which there exists a single break point that simultaneously breaks all feedback loops. Fig. 9 shows an example of such a circuit. It contains two feedback loops, which can both be broken at the X [either if $C_{gd}(M1) = C_{gd}(M2) = 0$ or if nonzero $C_{gd}(M1)$ and $C_{gd}(M2)$ are included in $Z1$ and $Z3$, respectively]. In general, suppose there are n feedback loops with at least one common break point. To analyze the small-signal stability of such a network, pick one controlled source from each loop, and call the values of those n selected controlled sources $k_m, m = 1, 2, \dots, n$. Also, assume that the circuit reduces to a single-loop network when all of the n selected controlled sources are set to zero except one, i.e., the circuit is single loop with respect to k_m if $k_i = 0$ for all $i \neq m$. Under these assumptions, Appendix A shows that the stability of the system is determined by the zeros of

$$1 + \sum_{m=1}^n RR_m(s) = 1 + RR_{ML}(s) \quad (4)$$

where RR_m is the (single-loop) return ratio computed for k_m when the other $n - 1$ selected sources are set to zero. Since RR_m is a single-loop return ratio, it has only left-half plane poles. Therefore RR_{ML} also has only left-half plane poles because it is a sum of the RR_m . As a result, the system stability can be determined by examining the gain and phase margins of RR_{ML} as in (1). Appendix A shows that RR_{ML} can be found by simulating the return ratio as described in this paper at a break point that simultaneously breaks all feedback loops.

These two special cases, applied independently or together, allow the extension of the return-ratio simulation techniques reviewed in Section III to many practical, fully differential circuits whose half circuits are not single-loop feedback networks.

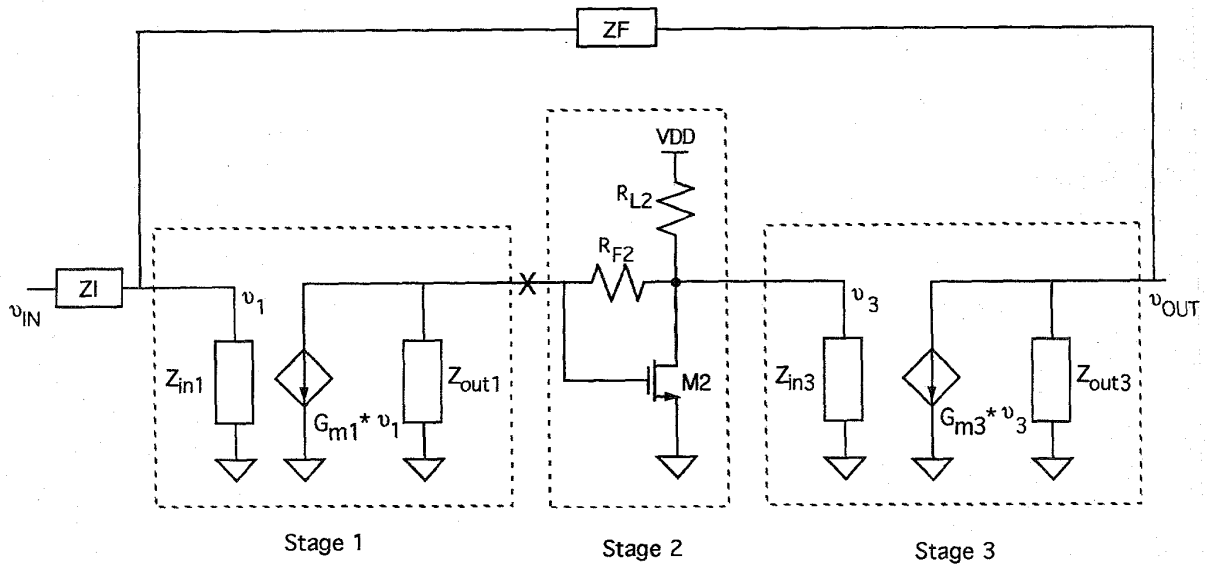


Fig. 8. A three-stage feedback circuit. The second stage consists of transistor M2 with local feedback through R_{F2} and $C_{gd}(M2)$ (which is not shown explicitly).

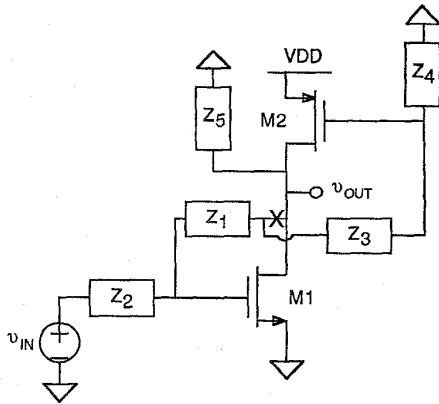


Fig. 9. An example of a circuit with multiple feedback loops and one break point that opens all loops.

V. SAMPLED-DATA CMSFB LOOPS

Switched-capacitor (SC) CMSFB is often used in fully differential SC circuits [21]. Fig. 10(a) shows an example of a circuit that uses a SC CMSFB network. It consists of two switched capacitors of value C_S , two hold capacitors of value C_H , and several switches that are controlled by a two-phase nonoverlapping clock (P1 and P2). Voltages V_{CM} and V_B are dc bias voltages; V_{CM} is the desired CM output voltage and V_B is the nominal bias voltage for node icm . Although all four capacitors sense the CM output at frequencies above dc, only the switched capacitors sense the dc component of the CM output. As a result, many clock cycles are required after the application of power for the circuit to converge to its steady-state, dc CM output voltage. On the other hand, to carry out stability simulations using ac analysis in SPICE, each switch must be either on or off. This means that the circuit used for SPICE simulation to determine stability will not also set up the CM dc operating point. To overcome this problem, a circuit

that is functionally equivalent to the SC network at dc can be used to force correct dc biasing during SPICE ac analysis.

An equivalent circuit can be found by analyzing the SC CMSFB loop. Fig. 10(b) shows a CM half circuit for the SC CMSFB portion of Fig. 10(a). Switched-capacitor C_S and hold capacitor C_H , together with the amplifier, form a SC integrator that is in a unity-gain feedback loop. If the dc CM output voltage, V_{OC} , is finite, C_S must not transfer charge onto C_H during P1 in steady state. This is true if the voltage across C_S during P2, $V_{CM} - V_B$, is equal to the voltage across C_S during P1, $V_{OC} - V_I$.¹ Therefore, an equivalent circuit must force

$$V_{OC} - V_I = V_{CM} - V_B, \quad (5a)$$

or

$$V_I = V_{OC} - V_{CM} + V_B. \quad (5b)$$

An equivalent circuit that satisfies (5b) is shown in Fig. 10(c). An inductor is connected between the icm node and the controlled sources that replicate the dc bias voltages. Because the dc voltage drop across the inductor is zero, (5b) is satisfied. When performing a DM simulation, the inductor value is unimportant since both sides of the inductor operate at ac ground when differential signals are applied. For a CM simulation, however, the inductor should be large enough to effectively disconnect the controlled sources from the icm node at all frequencies of interest.

The SC CMSFB loop provides one CM feedback path. Another CM feedback path is typically present, such as through ZF in Fig. 1. The special cases described in Section

¹In practice, the switches in Fig. 10(a) are realized with MOSFET's. This analysis ignores the dc leakage currents associated with the MOSFET junction diodes and any dc bias current that flows into amplifier A. Such dc currents cause $V_{OC} - V_I$ to differ from $V_{CM} - V_B$ by an amount that depends on the leakage currents, as shown in Appendix B. Also, the effects of clock feed-through and channel charge are ignored here and in Appendix B. They can cause an offset in the common-mode output voltage, which can be modeled by changing V_{CM} .

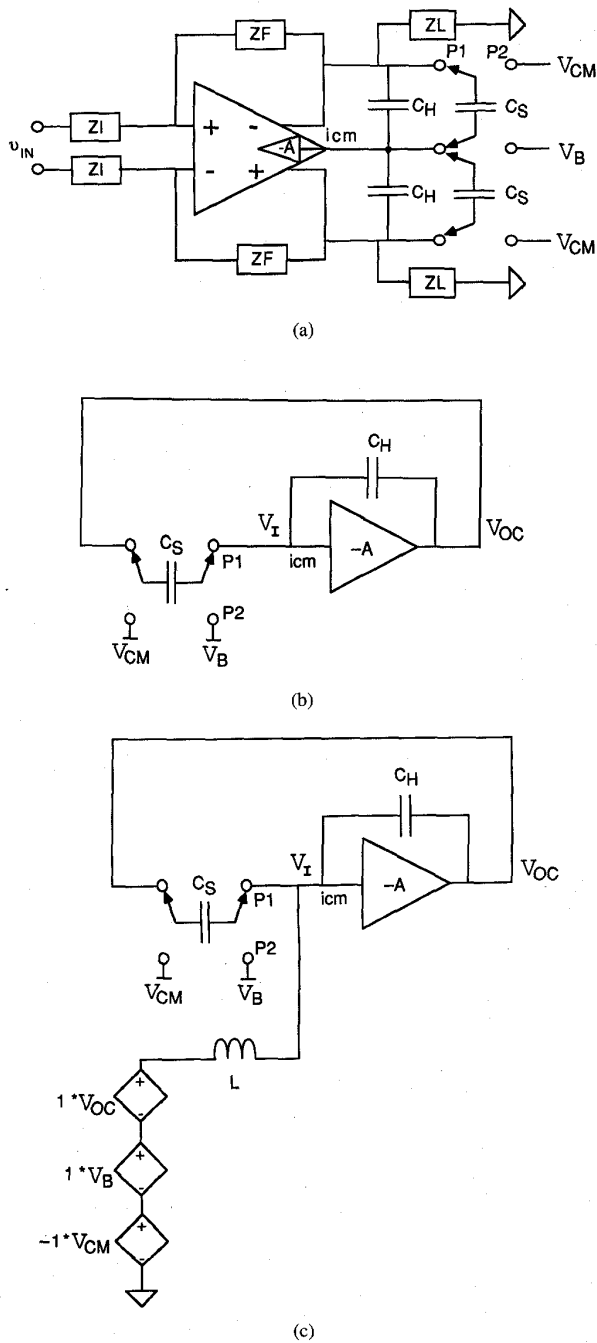


Fig. 10. (a) An op-amp feedback circuit showing the switched-capacitor CM sense feedback (CMSFB) loop. (b) The CM half circuit for the CMSFB loop. (c) The CM half circuit of (b) with an inductor and controlled sources added to provide dc feedback.

IV provide a means to determine stability in many practical cases with multiple CM loops.

VI. AN EXAMPLE

A fully differential sample-and-hold circuit is shown in Fig. 11. This circuit uses MOSFET switches controlled by nonoverlapping clocks P1 and P2 and has a SC CMSFB

network. When P2 is high, feedback is provided around the op amp through the C_F and C_H capacitors. The feedback has been broken at two symmetric break points, and the drive and measure terminals are labeled. To verify the RR simulations carried out by SPICE, a circuit that can be analyzed by hand is desired and the following assumptions are made:

- 1) The linear op-amp model in Fig. 12 is used.
- 2) Clock P1 is low, and clock P2 is high.
- 3) MOSFET switches that are off (operating in the cutoff region) are open circuits.
- 4) MOSFET switches that are on (operating in the triode region) are linear resistors. These include three transmission gates: two labeled as SF and connected to the C_F capacitors and one labeled as SI and connected to the C_I capacitors.

Under these conditions, $RR(DM)$ is

$$RR(DM) = \frac{2g_m Z_1 Z_2}{Z_1 + R_{ON}(SF) + \frac{1}{sC_F} + Z_2}, \quad (6)$$

where $Z_1 = (1/sC_{ioa})||[1/sC_I + R_{ON}(SI)/2]$ and $Z_2 = R_{od}||[1/s(C_{od} + C_H + C_L)]$. Also, $RR(CM)$ is:

$$RR(CM) = \frac{g_{mc} Z_{oc} Z_3}{2(Z_{oc} + Z_{od} + Z_3)} \cdot \frac{C_H}{C_H + \frac{C_{ic}}{2}}, \quad (7)$$

where $Z_{oc} = (2R_{oc})||[2/sC_{oc}]$, $Z_{od} = R_{od}||[1/sC_{od}]$, and $Z_3 = (1/sC'_L)||[1/sC_F + R_{ON}(SF) + 1/sC_{ioa}]$ with $C'_L = C_L + [C_H(C_{ic}/2)/(C_H + C_{ic}/2)]$.

Fig. 13 shows the SPICE simulation circuits, which use method 3 of Section III. The feedback circuit in Fig. 11 is shown simply as a box here with the drive and measure terminals labeled. As described in Section IV, an inductor connects controlled sources to the icm node in the SPICE files. When the test signals are differential, $RR(DM)$ is found [e.g., setting $v_{tp} = -v_{tn}$, $RR_V(DM) = -(v_{rp} - v_{rn})/(v_{dp} - v_{dn})$]. On the other hand, when the test signals are common mode, $RR(CM)$ is found [e.g., setting $v_{tp} = v_{tn}$, $RR_V(CM) = -(v_{rp} + v_{rn})/(v_{dp} + v_{dn})$]. Using the component values in the captions of Figs. 11 and 12, HSPICE [24] simulation results for $RR(DM)$ and $RR(CM)$ are plotted in Figs. 14 and 15, respectively. For the DM and CM cases, the maximum difference between the $|RR|$ from simulation and from the corresponding equation [(6) or (7)] is less than 0.002 dB for the frequencies plotted. The maximum difference between the phase of RR from simulation and the corresponding calculation is less than 0.02°.

HSPICE input and output files that simulate the return ratios for Fig. 11 are available through anonymous ftp at ftp://ftp.ece.ucdavis.edu/pub/sscrl/return_ratio. Information about the files is provided there in the README files.

VII. CONCLUSION

This paper has described frequency-domain SPICE simulation techniques that can be used to find the RR of the DM and

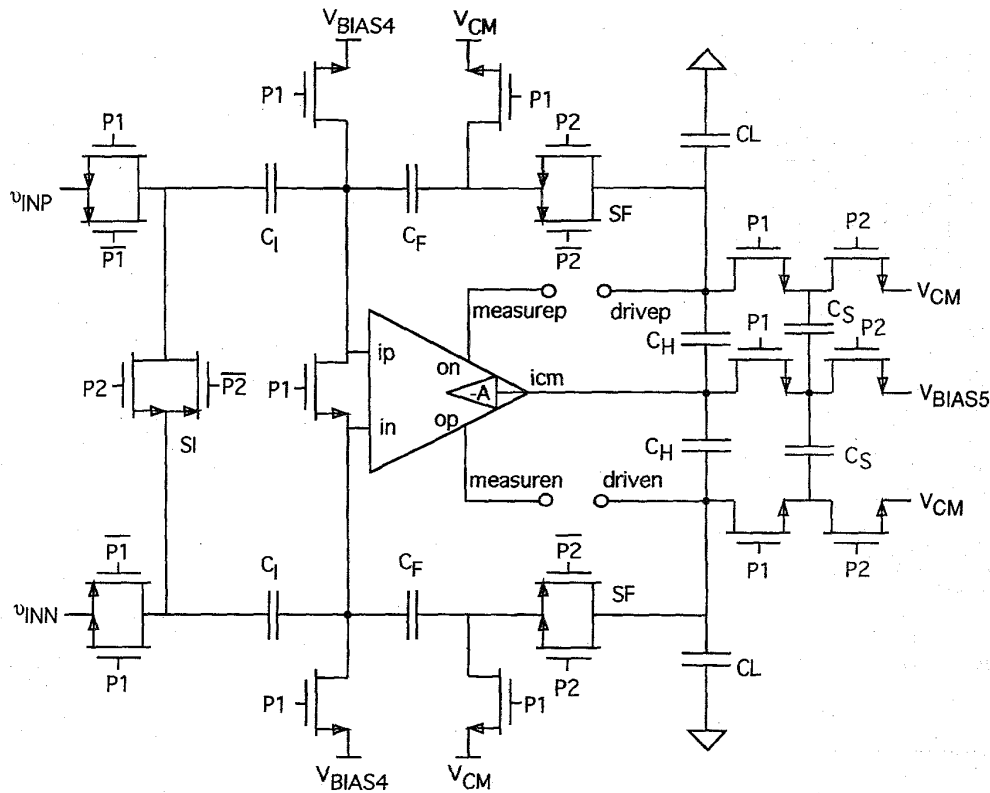


Fig. 11. An example fully differential sample-and-hold circuit with four terminals, labeled "measurep," "measuren," "drivep," and "driven." Component values are $C_F = 0.5$ pF, $C_I = 0.5$ pF, $C_L = 2$ pF, $C_H = 0.5$ pF, $C_S = 0.5$ pF. When P2 is high, $R_{ON}(SF) = 1$ k Ω and $R_{ON}(SI) = 1$ k Ω . Switches that are off are modeled as open circuits.

CM loops in fully differential feedback circuits. The stability of such circuits is determined by these two return ratios when:

1. the corresponding half circuits are single-loop feedback circuits, or
2. the corresponding half circuits are multiloop feedback circuits that conform to conditions given in Section IV.

The main advantage of these simulation techniques is that they can be used to measure the gain and/or phase margins, which can be used to determine stability in a small-signal sense. To determine whether the circuits are stable for large signals, the step response for a large input should also be observed in the time domain.

If a circuit is not perfectly balanced, then feedback loops that were not studied in this paper exist. In an unbalanced circuit, a CM op-amp input can produce a DM op-amp output, which may feed back a CM signal to the op-amp input. Such a feedback loop could cause instability. When the circuit is unbalanced due to typical component mismatches, however, these cross terms are small [11] and would rarely produce an instability. In the rare case where such an instability does exist, it could be found by a final time-domain SPICE simulation if the mismatch that causes nonzero cross terms is known.

Finally, limited node access in SPICE sometimes hinders the calculation of RR . This is because SPICE does not now allow access to nodes within a transistor model. For example, the gate-to-drain capacitance of a MOS transistor often provides a feedback path. To test the stability of this feedback path,

the capability of choosing a break point within the transistor model would be desirable.

APPENDIX A MULTIPLE FEEDBACK LOOP CIRCUITS WITH A COMMON BREAK POINT

This Appendix shows that, under certain conditions, the stability of a multiloop circuit can be determined by computing only one return ratio. The key condition is that the circuit contains n feedback loops that have at least one common break point that simultaneously breaks all n feedback loops. To analyze this problem, pick one controlled source from each loop and label the values of those n selected controlled sources k_i , $i = 1, 2, \dots, n$. In addition to the assumptions in Section II, assume here that:

- 1) There exists a single break point that simultaneously breaks all feedback loops.
- 2) The feedback circuit reduces to a single-loop network when all but one of the n selected controlled sources are set to zero, i.e., the circuit is single loop with respect to k_j if $k_i = 0$ for all $i \neq j$.
- 3) The current or voltage produced by each controlled source is a linear function of only one voltage or current in the network.

By Assumption 1, the signal flow graph for the feedback network can be drawn as in Fig. 16(a) [3], [22], where the signal at the common break point is y , a scalar voltage

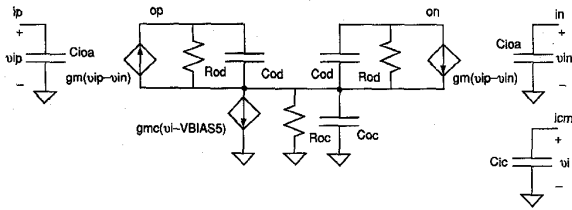


Fig. 12. A differential op-amp model for simulation and analysis of Fig. 11. Component values are $C_{ioa} = 1.25$ pF, $g_m = 1$ mS, $R_{od} = 1$ M Ω , $C_{od} = 1$ pF, $g_{mc} = 1$ mS, $R_{oc} = 1$ M Ω , $C_{oc} = 1$ pF, $C_{ic} = 1$ pF.

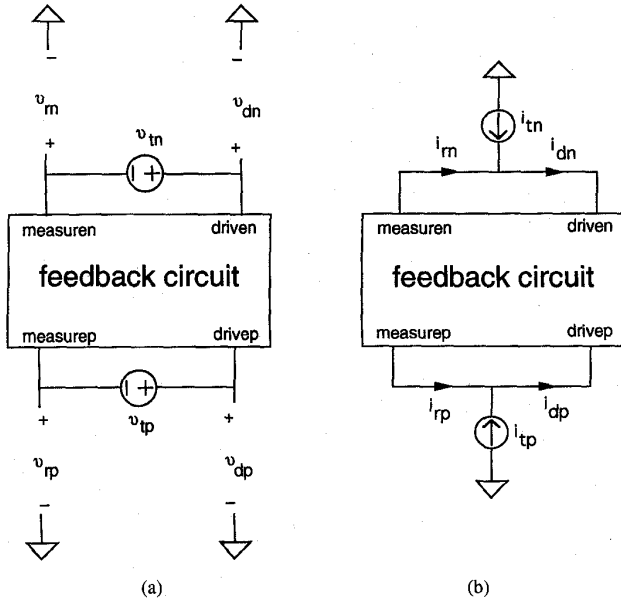


Fig. 13. Circuits for SPICE simulation of $RR(DM)$ and $RR(CM)$ in a differential circuit, using method 3 of Section III (see Fig. 4).

or current. In the following description of Fig. 16(a), let i represent an index ranging from 1 to n . Then:

- 1) \mathbf{p} is a $n \times 1$ vector in which each element, p_i , is the control signal (voltage or current) associated with the controlled source, k_i .
- 2) \mathbf{K} is a $n \times n$ matrix that maps \mathbf{p} to \mathbf{s} by $\mathbf{s} = \mathbf{K}\mathbf{p}$. By Assumption 3, \mathbf{K} is a diagonal matrix whose diagonal values are k_i , $i = 1, 2, \dots, n$.
- 3) \mathbf{s} is a $n \times 1$ vector in which each element, s_i , is the signal (voltage or current) that is directly controlled by k_i .
- 4) The signal flow from \mathbf{s} to \mathbf{y} is described by $\mathbf{y} = \mathbf{a}^T \mathbf{s}$, where \mathbf{a}^T is the transpose of \mathbf{a} .
- 5) The signal flow from \mathbf{y} to \mathbf{p} is given by $\mathbf{p} = -\mathbf{h}\mathbf{y}$, where \mathbf{h} is $n \times 1$.
- 6) The feedback loop is from \mathbf{p} to \mathbf{s} , through \mathbf{y} , and back to \mathbf{p} .

The transfer function matrix from \mathbf{in} to \mathbf{out} in Fig. 16(a) is [3]

$$\mathbf{CK}[\mathbf{I}_n + \mathbf{ha}^T \mathbf{K}]^{-1} \mathbf{B} + \mathbf{D}, \quad (A1)$$

where \mathbf{B} , \mathbf{C} , and \mathbf{D} are matrices that are determined by the circuit [3], and \mathbf{I}_n is the $n \times n$ identity matrix. Equation (A1) is the multidimensional extension of (1). The matrix

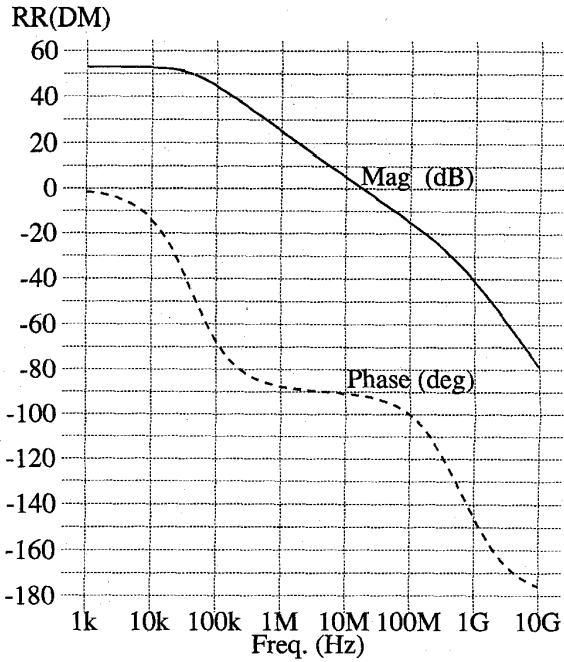


Fig. 14. Plots of HSPICE simulation results for the magnitude and phase of $RR(DM)$.

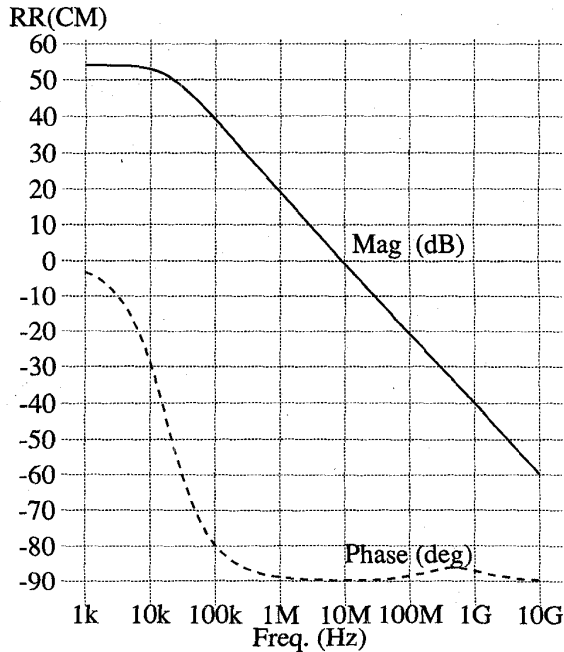


Fig. 15. Plots of HSPICE simulation results for the magnitude and phase of $RR(CM)$.

\mathbf{D} is the forward transmission when all $k_i = 0$. The terms \mathbf{CKB} give the forward gain through the controlled sources, and $[\mathbf{I}_n + \mathbf{ha}^T \mathbf{K}]^{-1}$ is analogous to $1/(1 + RR)$. The stability of the feedback circuit is determined by the zeros of [3]

$$\det[\mathbf{I}_n + \mathbf{ha}^T \mathbf{K}], \quad (A2)$$

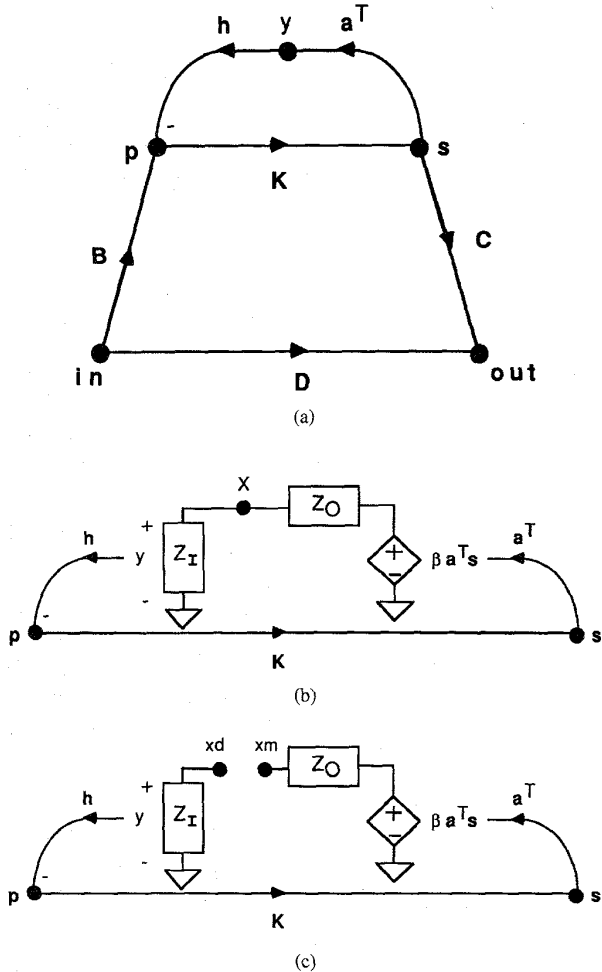


Fig. 16. (a) Signal-flow diagram for a network with multiple feedback loops and a common break point. (b) A model for the network at node X, when the signal y is a voltage. (c) The feedback is broken at node X.

which are the poles of the transfer function. The product $\mathbf{h}\mathbf{a}^T\mathbf{K}$ is a $n \times n$ matrix. Renaming the product $\mathbf{a}^T\mathbf{K} = (a_1k_1, a_2k_2, \dots, a_nk_n) = \mathbf{g}^T$ and using the fact that $\det[\mathbf{I}_n + \mathbf{Q}_{n \times m}\mathbf{R}_{m \times n}] = \det[\mathbf{I}_m + \mathbf{R}_{n \times m}\mathbf{Q}_{m \times n}]$ [23], (A2) can be simplified:

$$\begin{aligned} \det[\mathbf{I}_n + \mathbf{h}\mathbf{a}^T\mathbf{K}] &= \det[\mathbf{I}_n + \mathbf{h}\mathbf{g}^T] \\ &= \det[\mathbf{I}_1 + \mathbf{g}^T\mathbf{h}] \\ &= 1 + \mathbf{g}^T\mathbf{h}. \end{aligned} \quad (\text{A3})$$

The last equality follows because the determinant of a scalar equals that scalar. The term $1 + \mathbf{g}^T\mathbf{h}$, which appears in the denominator of the transfer function, has two important properties. First, the scalar $\mathbf{g}^T\mathbf{h}$ is equivalent to the usual return ratio since the poles of the transfer function are the zeros of $1 + \mathbf{g}^T\mathbf{h}$. Second, $\mathbf{g}^T\mathbf{h} = a_1k_1h_1 + a_2k_2h_2 + \dots + a_nk_nh_n$ is the sum of the n return ratios associated with the n single-loop feedback loops. This second property follows because the m th term in $\mathbf{g}^T\mathbf{h}$, $a_mk_mh_m$, is the return ratio for k_m with all other controlled sources set to zero.

Next, it will be shown that $\mathbf{g}^T\mathbf{h}$ can be found by breaking the multiloop feedback circuit at the common break point,

computing RR_I and RR_V , and combining them according to (2) to find the return ratio for the multiloop circuit,² $RR_{ML} = \mathbf{g}^T\mathbf{h}$. Fig. 16(b) shows the feedback network of Fig. 16(a) with a circuit model shown at the break point, which is labeled as node X. Here, the signal y at the break is assumed to be a voltage. (A similar argument can be made if y is a current.) The circuit model used in Fig. 16(b) includes a Thevenin equivalent circuit that drives node X and an impedance Z_I to ground that is the impedance seen looking to the left of node X. The controlled voltage source in Fig. 16(b) outputs $\beta\mathbf{a}^T\mathbf{s}$. This factor $\beta = (Z_I + Z_O)/Z_I$ compensates for the effect of the $Z_I - Z_O$ voltage divider to give $y = \mathbf{a}^T\mathbf{s}$. Fig. 16(c) shows the feedback broken at node X. The right-hand node is labeled xm ; the left-hand node is labeled xd . The open-circuit voltage at xm is $\beta\mathbf{a}^T\mathbf{s}$. When a test voltage v_t drives node xd , $\mathbf{p} = -\mathbf{h}v_t$ and $\mathbf{s} = \mathbf{K}\mathbf{p} = \mathbf{K}\mathbf{h}v_t$. Therefore, the return voltage at xm is

$$v_r = -\beta\mathbf{a}^T\mathbf{K}\mathbf{h}v_t, \quad (\text{A4})$$

and

$$\begin{aligned} RR_V &= -\frac{v_r}{v_t} \\ &= \beta\mathbf{a}^T\mathbf{K}\mathbf{h}. \end{aligned} \quad (\text{A5})$$

When a test current i_t drives node xd , the voltage developed at xd is $v_L = Z_I i_t$ and $\mathbf{p} = -\mathbf{h}v_L$. The short-circuit return current from node xm to ground is the voltage $\beta\mathbf{a}^T\mathbf{s} = \beta\mathbf{a}^T\mathbf{K}\mathbf{p}$ divided by Z_O ,

$$i_r = -\frac{\beta\mathbf{a}^T\mathbf{K}\mathbf{h}Z_I}{Z_O} i_t. \quad (\text{A6})$$

Therefore,

$$\begin{aligned} RR_I &= -\frac{i_r}{i_t} \\ &= \frac{\beta\mathbf{a}^T\mathbf{K}\mathbf{h}Z_I}{Z_O}. \end{aligned} \quad (\text{A7})$$

When these two quantities are combined according to (2), the result is

$$\begin{aligned} RR_{ML} &= \left[\frac{1}{RR_V} + \frac{1}{RR_I} \right]^{-1} \\ &= \left[\frac{1}{\beta\mathbf{a}^T\mathbf{K}\mathbf{h}} + \frac{1}{\frac{\beta\mathbf{a}^T\mathbf{K}\mathbf{h}Z_I}{Z_O}} \right]^{-1} \\ &= \mathbf{a}^T\mathbf{K}\mathbf{h} \left[\frac{1}{\beta} + \frac{1}{\frac{\beta Z_I}{Z_O}} \right]^{-1} \\ &= \mathbf{a}^T\mathbf{K}\mathbf{h} \left[\frac{Z_I}{Z_I + Z_O} + \frac{Z_O}{Z_I + Z_O} \right]^{-1} \\ &= \mathbf{a}^T\mathbf{K}\mathbf{h}, \end{aligned} \quad (\text{A8})$$

which is the desired result.

²The proof is given here only for (2). Similar steps will show that (3) can also be used to find RR_{ML} .

For example, consider the circuit with two feedback loops in Fig. 9. For simplicity, assume that the small-signal transistor model consists only of a transconductance ($i_d = g_m v_{gs}$). (All other small-signal-model elements can be absorbed into the impedances $Z_1 Z_5$.) Each feedback loop includes a controlled source associated with one transistor. Let $k_1 = g_{m1}$ and $k_2 = g_{m2}$. The circuit satisfies all the assumptions listed at the beginning of this appendix when the feedback loops are broken at the X. Therefore, the return ratio computed according to (2) [or (3), see fn. 2] at break point X is sufficient for testing stability, and this total return ratio is equal to the sum of the return ratios for the two controlled sources, each computed when the other controlled source is zero. To verify these statements, the transfer function for the circuit is computed first, and it is

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1} Z_L \frac{Z_1}{Z_1 + Z_2} + \frac{Z_L}{Z_1 + Z_2}}{1 + g_{m1} Z_L \frac{Z_2}{Z_1 + Z_2} + g_{m2} Z_L \frac{Z_4}{Z_3 + Z_4}}, \quad (\text{A9})$$

where $Z_L = Z_5 || (Z_1 + Z_2) || (Z_3 + Z_4)$. The return ratio for g_{m1} with $g_{m2} = 0$ is

$$RR(g_{m1} \text{ with } g_{m2} = 0) = g_{m1} Z_L \frac{Z_2}{Z_1 + Z_2}, \quad (\text{A10})$$

and the return ratio for g_{m2} with $g_{m1} = 0$ is

$$RR(g_{m2} \text{ with } g_{m1} = 0) = g_{m2} Z_L \frac{Z_4}{Z_3 + Z_4}. \quad (\text{A11})$$

The denominator of (A9) is one plus the sum of the two return ratios in (A5) and (A6).

RR_{ML} will now be found by computing RR_I and RR_V . Breaking at the X allows computation of the two return ratios, and the results are

$$RR_I = (Z_1 + Z_2) || (Z_3 + Z_4) \cdot \left[g_{m1} \frac{Z_2}{Z_1 + Z_2} + g_{m2} \frac{Z_4}{Z_3 + Z_4} \right], \quad (\text{A12})$$

$$RR_V = Z_5 \left[g_{m1} \frac{Z_2}{Z_1 + Z_2} + g_{m2} \frac{Z_4}{Z_3 + Z_4} \right]. \quad (\text{A13})$$

When (A12) and (A13) are combined according to (2), the RR for this multiple-loop circuit is

$$RR_{ML} = \left[\frac{1}{RR_I} + \frac{1}{RR_V} \right]^{-1} = g_{m1} Z_L \frac{Z_2}{Z_1 + Z_2} + g_{m2} Z_L \frac{Z_4}{Z_3 + Z_4}, \quad (\text{A14})$$

which equals the sum of (A10) and (A11) and equals the denominator of (A9) minus 1.

A direct calculation of RR_{ML} can be carried out using $RR_{ML} = \mathbf{g}^T \mathbf{h} = \mathbf{a}^T \mathbf{K} \mathbf{h}$. The controlled sources in the circuit are described by $i_{d1} = g_{m1} v_{gs1}$ and $i_{d2} = g_{m2} v_{gs2}$; therefore, $\mathbf{p}^T = (v_{gs1}, v_{gs2})$ and $\mathbf{s}^T = (i_{d1}, i_{d2})$. The matrix of control

values is

$$\mathbf{K} = \begin{bmatrix} g_{m1} & 0 \\ 0 & g_{m2} \end{bmatrix}. \quad (\text{A15})$$

With $y = v_{out}$, it follows that $\mathbf{a}^T = (Z_L, Z_L)$ and $\mathbf{h}^T = [Z_2/(Z_1 + Z_2), Z_4/(Z_3 + Z_4)]$, and therefore,

$$RR_{ML} = \mathbf{a}^T \mathbf{K} \mathbf{h} = g_{m1} Z_L \frac{Z_2}{Z_1 + Z_2} + g_{m2} Z_L \frac{Z_4}{Z_3 + Z_4}, \quad (\text{A16})$$

in agreement with the previous calculations.

APPENDIX B DERIVATION OF AN EQUIVALENT CIRCUIT FOR THE SC CMSFB LOOP AT DC

The analysis in Section V ignores the dc bias current that flows into the amplifier A and the dc leakage current associated with the reverse-biased source and drain junctions of the MOSFET's that act as the switches in Fig. 10. Furthermore, the analysis in Section V ignores the parasitic capacitance on the input of the amplifier because this capacitance is irrelevant when the input bias current and the leakage currents are zero. Fig. 17(a) shows the CM half circuit for Fig. 10(b) where the ideal switches have been replaced by MOS transistors and the amplifier input capacitance, C_P , is included. The transistor dimensions are those associated with the CM half circuit. Fig. 17(b) redraws this CM half circuit. Here the transistors are modeled by ideal switches, and two current sources that represent the drain- or source-bulk leakage currents that affect this analysis are shown. The leakage current of the drain-bulk junction of M2 is I_{J1} in Fig. 17(b). The leakage currents of the source-bulk junction of M2 and of the drain-bulk junction of M4 are lumped together into I_{J2} . All other leakage currents are supplied by a voltage source or by the op-amp output and therefore do not affect this analysis. (Any bias current that flows into the $-A$ amplifier can be lumped into I_{J1} .)

The charge-balance equation in Fig. 17(b) at time $n + 1$, which corresponds to the end of P1, is

$$\begin{aligned} (C_S + C_H)[v_{OC}(n+1) - v_I(n+1)] \\ + C_P[0 - v_I(n+1)] = \\ C_S[V_{CM} - V_B] + C_H[v_{OC}(n+1/2) - v_I(n+1/2)] \\ + C_P[0 - v_I(n+1/2)] + \frac{(I_{J1} + I_{J2})T}{2}, \quad (\text{B1}) \end{aligned}$$

where T is the period of the sampling clock and $T/2$ is the time P1 or P2 is high (assuming a negligible nonoverlap time). The last term on the right is a function of the leakage currents I_{J1} and I_{J2} , and it accounts for the currents flowing through the capacitors during P1. At time $n + 1/2$, which corresponds to the end of P2, the charge-balance equation is

$$\begin{aligned} C_H[v_{OC}(n+1/2) - v_I(n+1/2)] + C_P[0 - v_I(n+1/2)] \\ = C_H[v_{OC}(n) - v_I(n)] + C_P[0 - v_I(n)] + \frac{I_{J1}T}{2}. \quad (\text{B2}) \end{aligned}$$

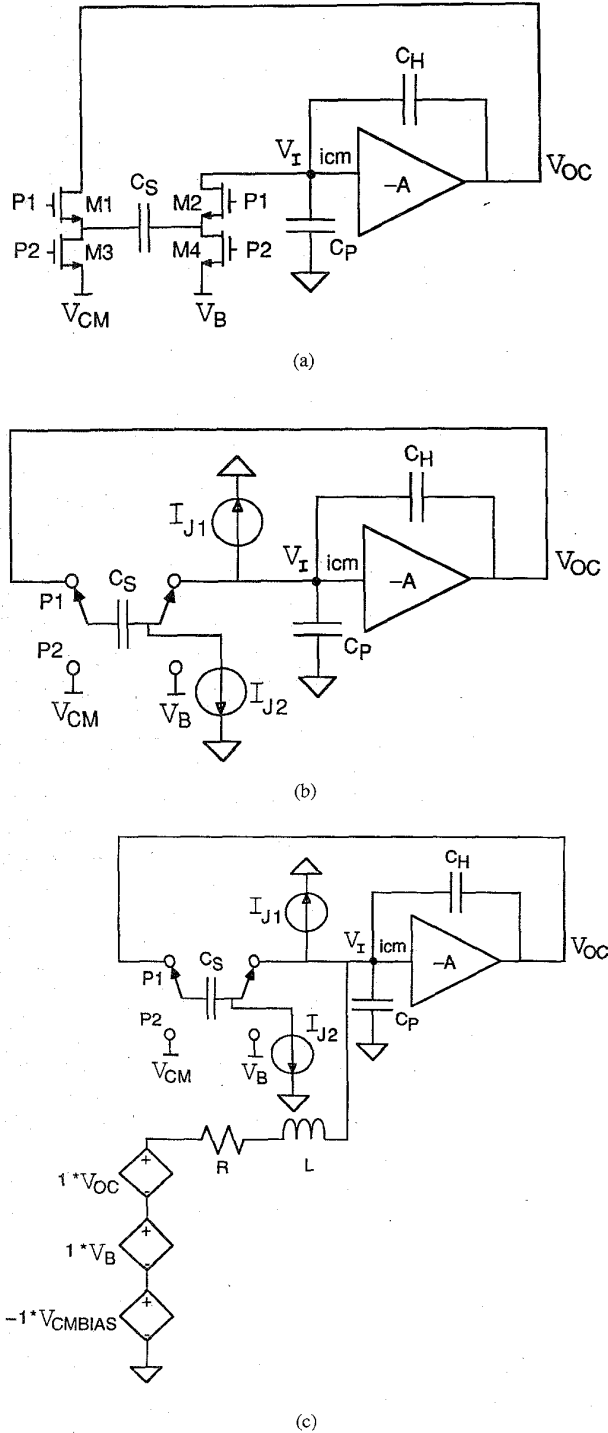


Fig. 17. (a) The CM half circuit of Fig. 10(b) showing the MOSFET switches and the parasitic capacitance on the amplifier input (C_P). (b) (a) with ideal switches in place of the transistors but including current sources I_{J1} and I_{J2} to model the key leakage currents of the MOSFET source and drain junction diodes. (c) Fig. 10(c) with a resistor R added to adjust V_I due to leakage currents.

The last term on the right accounts for the current I_{J1} flowing through the capacitors during P2. (Current I_{J2} is shunted to V_B during P2.) The next step in finding the dc solution during

P1 is to substitute (B2) into (B1) to yield

$$(C_S + C_H)[v_{OC}(n+1) - v_I(n+1)] = C_S[V_{CM} - V_B] + C_H[v_{OC}(n) - v_I(n)] + \frac{I_{J1}T}{2} + \frac{(I_{J1} + I_{J2})T}{2}. \quad (B3)$$

When the circuit has reached steady state (i.e., $n \rightarrow \infty$), each node voltage at time n equals the corresponding node voltage at time $n+1$. For example, $v_{OC}(n+1)|_{n \rightarrow \infty} = v_{OC}(n)|_{n \rightarrow \infty}$. This condition, when applied to (B3), gives

$$v_{OC}(\infty) - v_I(\infty) = V_{CM} - V_B + \frac{(2I_{J1} + I_{J2})T}{2C_S} \quad (B4)$$

on P1. This equation is similar to (5a) with the addition of the current-dependent error:

$$\Delta V_1 = \frac{(2I_{J1} + I_{J2})T}{2C_S}. \quad (B5)$$

In steady state, the error, ΔV_1 , is independent of C_H and C_P because the dc leakage current flows only through the switched capacitor, C_S . This error can be included in the simulation by adding a resistor R in series with the inductor as shown in Fig. 17(c). Since C_S is not switched during ac simulations, both currents I_{J1} and I_{J2} flow through R when P1 is high. Let $R = R_{P1}$ here, which represents R on P1. To develop a voltage drop of ΔV_1 ,

$$(I_{J1} + I_{J2})R_{P1} = \frac{(2I_{J1} + I_{J2})T}{2C_S}, \quad (B6a)$$

or

$$R_{P1} = \frac{(2I_{J1} + I_{J2})T}{2C_S(I_{J1} + I_{J2})} = \frac{(2 + \frac{I_{J2}}{I_{J1}})T}{2C_S(1 + \frac{I_{J2}}{I_{J1}})}. \quad (B6b)$$

Note that R_{P1} depends on the current ratio I_{J2}/I_{J1} . If $V_I \approx V_B$, then the diode voltages are similar and therefore I_{J2}/I_{J1} is about equal to the ratio of the junction areas. For example, if M1–M4 in Fig. 17(a) are identical, $I_{J2}/I_{J1} \approx 2$. This area ratio, when substituted into (B6b), leads to a simplified equation for R_{P1} ,

$$R_{P1} \approx \frac{4T}{6C_S}. \quad (B7)$$

The dc solution at the end of P2 can be found using (B1) and (B2), noting that $v_{OC} = -Av_I$ (always), and letting $n \rightarrow \infty$, which means that each node voltage at time $n - 1/2$ equals the corresponding node voltage at time $n + 1/2$. The result is

$$v_{OC}(\infty + 1/2) - v_I(\infty + 1/2) = V_{CM} - V_B + \frac{(2I_{J1} + I_{J2})T}{2C_S} + \frac{I_{J1}T}{2\left(C_H + \frac{C_P}{1+A}\right)}. \quad (B8)$$

This equation is similar to (5a) with the addition of the current-dependent error:

$$\Delta V_2 = \frac{(2I_{J1} + I_{J2})T}{2C_S} + \frac{I_{J1}T}{2\left(C_H + \frac{C_P}{1+A}\right)} = \Delta V_1 + \frac{I_{J1}T}{2C_H}, \quad (B9)$$

where $C'_H = C_H + C_P/(1 + A)$. The error, ΔV_2 , differs from ΔV_1 in (B5) by an amount that depends on C_H and C_P because I_{J1} flows through C_H in parallel with $C_P/(1 + A)$ during P2, which can be seen by applying the Miller effect in reverse on C_P . Again, this error can be generated in the simulation by the resistor R in series with the inductor in Fig. 17(c). Here, let $R = R_{P2}$, which represents R on P2. Since $I_{J1}R_{P2} = \Delta V_2$, R_{P2} should be chosen as:

$$R_{P2} = \frac{\left(2 + \frac{I_{J2}}{I_{J1}}\right)T}{2C_S} + \frac{T}{2C'_H}. \quad (\text{B10})$$

Using $I_{J2}/I_{J1} = 2$ as above gives

$$R_{P2} = \frac{4T}{2C_S} + \frac{T}{2C'_H}. \quad (\text{B11})$$

Although the exact value of R_{P2} depends on both C_P and A (which are both unknown in most practical cases), the dependence is small if $C_P/(1 + A) \ll C_H$. Furthermore, the effect of these leakage currents can be completely ignored in most cases. For example, with a (large) $I_{J1} = 1$ nA and $I_{J2} = 2I_{J1} = 2$ nA and $C_S = 1$ pF, (B5) gives

$$\begin{aligned} \Delta V_1 &= \frac{(2I_{J1} + I_{J2})T}{2C_S} \\ &= (2 \text{ V/msec})T. \end{aligned} \quad (\text{B12})$$

If $T = 1$ μsec , $\Delta V_1 = 2$ mV, which is insignificant in most cases. However, for the same currents with $C_S = 0.1$ pF and $T = 100$ μsec , then $\Delta V_1 = 2$ V, which is a voltage drop that should not be neglected.

Finally, note that Fig. 17(c) shows a CM half circuit, and the desired equivalent resistance would actually have to be included in Fig. 10(a) for simulation. A resistance of $R/2$ used in Fig. 10(a) is equivalent to the resistance R in the CM half circuit in Fig. 17(c). (Halving the resistance in the balanced circuit holds the error constant because the leakage currents in the balanced circuit are double those in the CM half circuit.)

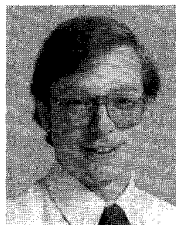
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Transactions Briefs

A New IIR Echo Canceller Structure

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Abstract—A new recursive adaptive filter structure is proposed, which is composed of a transversal block and a cascade block connected in series. The transversal block implements the zeros of the system function and provides an easy gradient estimation and robust convergence. The cascade block implements the poles of the system function and allows an easy control of the poles positions to ensure stability. The coefficients are updated using either the LMS algorithm, which is robust and simple, or the AFM algorithm [12]–[14], which, in some cases, gives a better performance. Computer simulations indicate that, in some cases, the new echo canceller shows a better performance than conventional realizations.

I. INTRODUCTION

Conventional echo cancellers are nonrecursive structures based on transversal (FIR) adaptive filters; very high orders are often required, specially when they have to realize a long impulse response.

It is well known that low order recursive structures (usually IIR) can have a frequency response comparable to that of a nonrecursive structure of much higher order and are usually preferred in the realization of nonadaptive filters. This has motivated an interest in the use of recursive adaptive structures, not only in echo cancelling [1], [2], but also in other areas [3]–[9]. However, recursive structures, when used in the adaptive mode, have two important limitations with respect to nonrecursive structures: they require control of the poles positions in order to avoid instability, and they may have convergence difficulties caused by error surfaces with local minima. If these limitations could be attenuated or eliminated, adaptive recursive structures might become advantageous with respect to conventional (nonrecursive) realizations. In fact, local minima can be avoided by using recursive structures of an adequate order [10] and control of the poles positions can be easily achieved with suitable structures.

The system identification problem corresponding to the proposed echo canceller is depicted in Fig. 1, where $H(z) = A(z)/B(z)$ is the echo path system function, $\hat{H}(z) = \hat{A}(z)/\hat{B}(z)$ is the estimate of $H(z)$ provided by the adaptive recursive filter, x_k denotes the transmitted data signal, e_k is the echo resulting from x_k , \hat{e}_k is the echo estimate, r_k denotes the received data from the far-end transmitter plus noise, and y_k is the system identification error and also the echo canceller output.

In this brief, we propose a new recursive structure for the realization of $\hat{H}(z)$, the hybrid-series structure, which, in some cases, is advantageous, not only with respect to the conventional adaptive transversal structure, but also with respect to some recursive structures. Only gradient algorithms are considered, for their simplicity and robustness.

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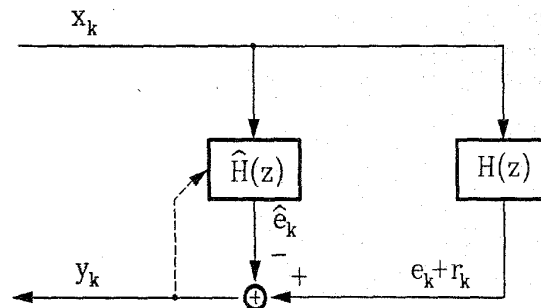


Fig. 1. Basic block diagram of the echo canceller.

II. THE HYBRID-SERIES STRUCTURE

The new structure proposed here combines two distinct blocks in series: a transversal filter, which is associated with the numerator of the system function and a cascade of first-order recursive sections. Since the structure is the series connection of a nonrecursive (FIR) block and a recursive block, the name *hybrid-series* is used. The FIR block allows an easy gradient estimation and a robust convergence. The cascade of first-order sections provides easy control of the poles positions to ensure stability: all the denominator coefficients must have magnitudes smaller than 1, in order for the poles to remain inside the unit circle.

The use of first-order sections implies real poles. This may be a limitation in some applications, but it is not a serious drawback in echo cancellation, since there is no reason to expect the echo path to have a highly frequency-selective response. This has been confirmed experimentally for some hybrids currently used in data modems. If the echo path system function has complex poles, the required response may be closely approximated by assuming an echo canceller of order suitably higher than that of the echo path. Fig. 2 shows the proposed structure for $N = M = 3$. The corresponding system function is, thus

$$\hat{H}(z) = \frac{\hat{A}(z)}{\hat{B}(z)} = \frac{\sum_{i=0}^N \hat{a}_i z^{-i}}{\prod_{i=1}^M (1 + \hat{b}_i z^{-i})} \quad (1)$$

Denoting by \hat{c}_i any of the echo canceller parameters, the LMS algorithm [11, p. 100] to update it can be expressed as follows

$$\begin{aligned} \hat{c}_i(k+1) &= \hat{c}_i(k) - \mu \frac{\partial y_k^2}{\partial \hat{c}_i} = \hat{c}_i(k) + 2\mu y_k \frac{\partial \hat{e}_k}{\partial \hat{c}_i} \\ &= \hat{c}_i(k) + 2\mu y_k \psi_{\hat{c}_i}(k) \end{aligned} \quad (2)$$

where $y_k = e_k + r_k - \hat{e}_k$, μ is the step-size coefficient and $\psi_{\hat{c}_i}(k) = \partial \hat{e}_k / \partial \hat{c}_i$. The z -transform of $\psi_{\hat{c}_i}(k)$ is

$$\Psi_{\hat{c}_i}(z) = \frac{\partial \hat{E}(z)}{\partial \hat{c}_i} = X(z) \frac{\partial \hat{H}(z)}{\partial \hat{c}_i} \quad (3)$$

where $\hat{E}(z)$ and $X(z)$ are the z -transforms of \hat{e}_k and x_k , respectively. For the numerator coefficients of $\hat{H}(z)$ ($\hat{c}_i = \hat{a}_i$), and the denominator coefficients ($\hat{c}_i = \hat{b}_i$), we obtain, respectively,

$$\Psi_{\hat{a}_i}(z) = \frac{\partial \hat{E}(z)}{\partial \hat{a}_i} = X(z) z^{-i}, \quad i = 0, 1, \dots, N \quad (4)$$